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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,853	12/02/2003	Scott Fairbanks	6429P001	5587

8791 7590 04/17/2006

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EXAMINER	
NGUYEN, HAI L	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

B/c

Office Action Summary	Application No.	Applicant(s)	
	10/726,853	FAIRBANKS, SCOTT	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *39-76* is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment received on 02/01/2006 has been reviewed and considered with the following results:

As to the objection to claim 33, Applicant's amendments have overcome the objection, as such; the objection has been withdrawn.

As to the prior art rejections to claims 1-38, the arguments and/or comments by the Applicant have been carefully reviewed, but are not persuasive because the claimed limitations are clearly anticipated by the cited reference. The arguments supporting the previous rejections are addressed in detail below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 4-7, 10-12, 14-22, 24-31, and 33-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Fairbanks (US 6,191,658; previously cited).

With regard to claim 1, Fairbanks discloses in Fig. 3A an apparatus comprising a clock generator, distributed over an integrated circuit, including a plurality of cells (200A-200D) each coupled to multiple adjacent ones of the plurality of cells by different clock wires, wherein, for

each of the plurality of clock wires, the cell on one end generates the rising edge and the cell on the other end generates the falling edge.

With regard to claims 2, 4-7, and 10, the reference also meets the recited limitations in these claims.

With regard to claim 11, Fairbanks discloses in Fig. 3A an apparatus comprising a clock generator to generate a clock signal through the interaction of a plurality of cells (200A-200D) distributed in grid over an integrated circuit, wherein each of the plurality of cells is coupled to multiple adjacent complementary ones of the plurality of cells by different clock wires; and a plurality of sets of synchronous logic each coupled to a different one of the clock wires, wherein the plurality of sets of synchronous logic are interconnected.

With regard to claims 12 and 14-19, the reference also meets the recited limitations in these claims.

With regard to claim 20, at least the pull-up type cells or the pull-down type cells include initialization circuitry (see column 4, lines 14-27).

With regard to claim 21, Fairbanks discloses in Figs. 2A-3A an apparatus comprising a clock generator including a plurality of cells (200A-200D) distributed in grid over an integrated circuit, that collectively form an oscillator of the clock generator, wherein each of the plurality of cells oscillate dependent upon clock signals received from multiple of others of the plurality of cells; and a plurality of sets of synchronous logic (not shown, for example, computer systems or microprocessors), distributed over the integrated circuit, coupled to be clocked by the clock generator.

With regard to claims 22 and 24-29, the reference also meets the recited limitations in these claims.

With regard to claim 30, Fairbanks discloses in Fig. 3A an integrated circuit comprising a distributed clock generator including, a plurality of cells (200A-200D) that, responsive to an averaging of a previous clock edge produced by the plurality of cells, detect when to produce the next clock edge, and a plurality of clock wires each coupling together two of the plurality of cells such that the plurality of cells are coupled together in grid; and a plurality of sets state holding elements (back-to-back inverters connected) each having a clock input, each clock input of each of the sets coupled to a different one of the plurality of clock wires.

With regard to claims 31 and 34-38, the reference also meets the recited limitations in these claims.

With regard to claim 33, on any one of the pluralities of clock wires (i.e., from OA1 & OB1 to 200B), the current always travels in the same direction once the clock signal has been initialized.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3, 13, 23, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fairbanks in view of Graef (US 6,305,001; previously cited).

With regard to claim 3, the above discussed clock generator circuit of Fairbanks meets all of the claimed limitations except that Fairbanks does not disclose that the clock grid is three-dimensional. Graef teaches a similar clock generator circuit having three-dimensional grid (see column 13, lines 17-31). Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to utilize that teaching of Graef with the prior art by implementing the clock grid in three-dimensional in order to minimize chip area.

Claims 13, 23, and 32 are similarly rejected; note the above discussion with regard to claim 3.

6. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fairbanks.

The above-discussed clock generator circuit of Fairbanks meets all of the claimed limitations except that the shape is not specifically mentioned, such as irregular shape or one of a square and a rectangle. However, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention was made to change the shape of the clock grid circuit for meeting specific condition which is in each case optimally matched to its application. Since it has been held that discovering an optimum skill in the art. See *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

7. Applicant's first argument stating that Fairbanks fails to teach the limitations "wherein, for each of the plurality of clock wires, the cell on one end generates the rising edge and the cell on the other end generates the falling edge, as recited by claim 1". That argument is not persuasive because the claimed limitations "the cell on one end generates the rising edge and the

cell on the other end generates the falling edge," are clearly anticipated by the reference. For example, the cell on one end (at node 206A in Fig. 3A of Fairbanks) generates the rising edge and the cell on the other end (at node 206B) generates the falling edge. Therefore, the rejections of record are still believed to be proper and are therefore maintained as set forth above.

8. Applicant's second argument stating that Fairbanks fails to teach the limitations "wherein each of the plurality of cells is coupled to multiple adjacent complementary ones of the plurality of cells by different clock wires, as recited by claim 11". That argument is not persuasive because the claimed limitations "each of the plurality of cells is coupled to multiple adjacent complementary ones of the plurality of cells by different clock wires" are clearly anticipated by the reference. For example, the logic of node 206A of cell 200A (Fig. 3A of Fairbanks) changes to a logic High, which then causes the logics of nodes 206B and 204D of multiple adjacent complementary cells 200A and 200D respectively, changing to a logic Low. Thus indicating that the adjacent cell connected to any one cell is complementary to and not the same as that cell. Therefore, the rejections of record are still believed to be proper and are therefore maintained as set forth above.

9. Applicant's third argument stating that Fairbanks fails to teach the limitations "wherein each of the plurality of cells oscillate dependent upon clock signals received from multiple of others of the plurality of cells, as recited by claim 21". That argument is not persuasive because the claimed limitations "each of the plurality of cells oscillate dependent upon clock signals received from multiple of others of the plurality of cells" are clearly anticipated by the reference. For example, the cell 200D (Fig. 3A of Fairbanks) oscillates dependent upon clock signals received from others cells 200A and 200C (see column 3, line 20 through column 4, line 28).

10. Applicant's last argument stating that Fairbanks fails to teach that the cells are "responsive" to averaging of previous clock edge and "detect when to produce the next clock edge", as recited by claim 30 ". That argument is not persuasive because the claimed limitations are clearly anticipated by the reference. For example, the cell 200A (Fig. 3A of Fairbanks) oscillates dependent upon clock signals received from others cells 200D and 200C (see column 3, line 20 through column 4, line 28). In other words, the cells in Fig. 3A of Fairbanks collectively average previous clock edge produced by a plurality of cells and detect when to produce the next clock edge. Therefore, the rejections of record are still believed to be proper and are therefore maintained as set forth above.

Allowable Subject Matter

11. Claims 39-76 are allowed.

The prior art of record fails to disclose or fairly suggest a distributed clock generator (as shown in Figs. 6-7), and a method of use thereof, as recited in claims 39 and 75, having specific structural limitations such as comprising a plurality of cells (701-716) each including, a plurality of terminals, a cumulative clock edge detection circuit (601-604 in instant Fig. 6) coupled to the plurality of terminals and having an output (605), a delay/amplification circuit (606-608) coupled to the output of the cumulative clock edge detection circuit, and a driver circuit (609-612) coupled to the plurality of terminals and to the delay/amplification circuit; a plurality of clock wires (N, E, S, W), each of the plurality of clock wires coupling one of the plurality of terminals of one of the plurality of cells to one of the plurality of terminals of another of the plurality of cells.

The prior art of record fails to disclose or fairly suggest a distributed clock generator (as shown in Figs. 6-7), as recited in claim 52, having specific structural limitations such as comprising a plurality of cells (701-716) collectively having a plurality of terminal pairs, each of the plurality of terminal pairs (inputs of 601 & 603, and 602 & 604) including a charging terminal (inputs of 601 and 602) coupled to a discharging terminal (inputs of 603 and 604) to have generated there between a clock signal (605) having its two edges defined by alternating activation/deactivation of the charging terminal and the discharging terminal, the terminals of each of the plurality of terminal pairs being part of two different ones of the plurality of cells, the plurality of cells coupled together as a result of each being coupled to certain others of the plurality of cells by the plurality of terminal pairs; and being configured in combination with the rest of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose or fairly suggest a cell (as shown in Fig. 6) of distributed clock generator (Fig. 7), as recited in claim 62, having specific structural limitations such as comprising a set of terminals of the cell, each of the terminals in the set being one terminal of a different terminal pair, each of the terminal pairs (inputs of 601 & 603, and 602 & 604) including a charging terminal (inputs of 601 and 602) coupled to a discharging terminal (inputs of 603 and 604) to have generated there between a clock signal (605) having its two edges defined by alternating activation/deactivation of the charging terminal and the discharging terminal; a cumulative clock edge detection circuit (601-604) coupled to the set of terminals to determine a single clock edge transition time reflective of transitions of the clock signals on the terminals, a driver circuit (609-612) coupled to the set of terminals; and a delay/amplification circuit (606-608), coupled to an output of the cumulative clock edge detection circuit and to the

driver circuit, to cause another clock edge transition of the clock signals to substantially simultaneously occur some delay time after each of the single clock edge transition times.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HLN
April 11, 2006

Kenneth B. Wells
Primary Examiner